OSTIM TECHNICAL UNIVERSITY
FACULTY OF ENGINEERING

COURSE SYLLABUS FORM
2022-2023

Course Name	Course Code	Period	Hour	Apllication Hour	Lab Hour	Credit	ECTS
Int. to Logic Design	EEE207	Fall	3	0	0	3	3

Prerequisite	None
Language of Instruction	English
Course Status	Obligatory
Course Level	Undergraduate
Method of Teaching	In class lectures
Learning and Teaching Techniques of the Course	Lectures, Homeworks, Projects

Course Objective

The aim of this course is to introduce students digital-analog concepts, number systems, Boolean operations, combinational logic circuits, simplifications, Karnaugh map, sequential logic circuits, programmable devices, registers and counters, digital/analog and analog/digital conversion… and to prepare them for advanced courses in microprocessors, computer architecture and VLSI.

Learning Outcomes

	Upon successful completion, students will have the knowledge and skills to:			
1.	Interpret about the differences between between analog/digital signals			
2	Learn about the number systems and boolean algebraic operations			
3	Demonstrate understanding of combinational logic circuits functions			
4	Understand and describe sequential logic circuits functions			
5	Learn about programmable devices, registers and counters..			

Course Outline

This course is an introduction to Digital Design with Logic Design as the primary focus. Topics include digital-analog concepts, number systems, Boolean operations, combinational logic circuits, simplifications, K-map, sequential logic circuits, programmable devices, registers and counters, digital/analog and analog/digital conversions etc..

Weekly Topics and Releated Preparation Studies

Weeks	Topics	Preparation Studies
1	Digital-analog definitions	Chapter 1, Mano & Ciletti,6th Ed.
2	Number systems, Boolean operations, Logic gates	Chapter 2, Mano & Ciletti,6th Ed.
3	Number systems, Boolean operations, Logic gates	Chapter 2, Mano & Ciletti,6th Ed.
4	Simplification of Boolean functions, Karnaugh map	Chapter 3, Mano & Ciletti,6th Ed.
5	Simplification of Boolean functions, Karnaugh map	Chapter 3, Mano & Ciletti,6th Ed.
6	Simplification of Boolean functions, Karnaugh map	Chapter 3, Mano & Ciletti,6th Ed.
7	2 level implementations	Chapter 3, Mano & Ciletti,6th Ed.
8	**Midterm Exam**	
9	2 level implementations, Design of combinational circuits	Chapter 3, Mano & Ciletti,6th Ed.
10	2 level implementations, Design of combinational circuits	Chapter 3, Mano & Ciletti,6th Ed.
11	Design of combinational circuits	Chapter 4, Mano & Ciletti,6th Ed.
12	Design of combinational circuits	Chapter 4, Mano & Ciletti,6th Ed.
13	Sequential logic circuits, programmable devices, registers and counters.	Chapter 5, Mano & Ciletti,6th Ed.
14	Sequential logic circuits, programmable devices, registers and counters.	Chapter 5, Mano & Ciletti,6th Ed.
15	HDL principles, digital/analog and analog/digital conversion	Chapter 6, Mano & Ciletti,6th Ed.
16	**Final Exam**	

Textbook(s)/References/Materials:

M. Morris Mano and Michael D. Ciletti, Digital Design with an Introduction to the Verilog HDL, VHDL, and System Verilog, 6th Edition/Global Edition.

Assessment

Studies	Number	Contribution margin (%)
Active Participation		
Lab		
Application		
Field Study		
Course-Specific Internship (if any)		
Quizzes / Studio / Critical	2	25
Homework		
Presentation		
Projects		
Report		

Seminar			
Midterm Exams / Midterm Jury	1	35	
General Exam / Final Jury	1	40	
	Total		
Success Grade Contribution of Semester Studies		60	
Success Grade Contribution of End of Term		40	
	Total	100	

Course Category	
Basic Vocational Courses	x
Specialization/Field Courses	
Support Courses	
Communication and Management Skills Courses	
Transferable Skills Courses	

Relationship Between Course Learning Outcomes and Program Competencies						
No	**Learning Outcomes**	**Contribution Level**				
		1	**2**	**3**	**4**	**5**
1	Ability to apply knowledge of mathematics, science, and engineering				x	
2	Ability to design and conduct experiments and to analyze and interpret experimental results.					
3	Ability to design a system, component, and process according to specified requirements.				x	
4	Ability to work in teams in interdisciplinary areas.				x	
5	Ability to identify, formulate and solve engineering problems.				x	
6	Identifies, defines, formulates and solves complex network problems; chooses and applies analysis and modeling methods suitable for this purpose.					x
7	Develops, selects and uses modern techniques and tools necessary for the analysis and solution of complex problems encountered in Electrical and Electronics Engineering applications; uses required technologies effectively.					x

ECTS / Workload Table			
Activities	**Number**	**Duration (Hours)**	**Total Workload**
Course hours (Including the exam week: 16 x total course hours)	14	3	42
Laboratory			
Application			
Course-Specific Internship			
Field Study			
Study Time Out of Class	14	2	28
Presentation / Seminar Preparation			
Projects			
Reports			
Homeworks			
Quizzes / Studio Review	2	3	6
Preparation Time for Midterm Exams / Midterm Jury	1	12	12
Preparation Period for the Final Exam / General Jury	1	12	12
Total Workload	**(100/30=3,3)**		**100**